Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims of this application:

Listing of Claims:

1. (Currently Amended) A method of programming an electronic device comprising:

transferring ~~program~~ data information and address information included in program data provided from outside the electronic device to a buffer circuit coupled to a programmable memory in the electronic device ~~via a controller circuit,~~ without using Random Access Memory (RAM) and Read Only Memory (ROM) devices that are separate from ~~the~~ a programmable memory controller circuit, ~~that~~ wherein the programmable memory controller circuit controls programming of the programmable memory in the electronic device that is separate from a general operation processor circuit used to provide general operations of the electronic device subsequent to transferring ~~the program data~~ data information into the programmable memory;

transferring command information to the programmable memory controller circuit, wherein command information is used to generate control signals used in conjunction with data information and address information transferred to the buffer circuit, wherein the control signals are generated by the programmable memory controller circuit;

decoding addresses~~, within the controller circuit~~ received without passing through the general operation processor circuit, to determine that ~~the transferred data~~ data information transferred to the buffer circuit is directed to the programmable memory ~~mapped address to which the transferred data is to be programmed as specified in a head field and a command/address field data structure received by the controller circuit~~ mapped address information transferred to the buffer circuit;

asserting a signal to the general operation processor circuit, responsive to decoding the programmable memory mapped address by the programmable memory controller circuit, to prevent the general operation processor circuit from accessing the programmable memory

during transfer of ~~program~~ data information into the programmable memory;

transmitting an indication to outside the electronic device that the transfer of ~~program~~ data information to the programmable memory is complete; and then

de-asserting the signal to the general operation processor circuit to allow the general operation processor circuit to access the programmable memory.

Claims 2 (Canceled).

3. (Previously presented) The method according to Claim 1 wherein the RAM and ROM operate under control of the general operation processor circuit and not under the control of the controller circuit.

4. (Previously presented) The method according to Claim 1 wherein the step of transferring the program data further comprises transferring the program data via a Video Graphics Adapter (VGA) interface to the electronic device.

5. (Previously presented) The method according to Claim 1 wherein the step of transferring the program data further comprises transferring the program data via an Inter-Integrated Circuit interface to the electronic device.

Claim 6 (Canceled).

7. (Previously presented) The method according to Claim 1 wherein the general operation processor circuit accesses separate RAM and ROM to provide general operations of the electronic device.

Claims 8-9 (Canceled).

10. (Previously presented) The method according to Claim 1 further comprising:

transmitting a reset to the controller circuit to enable the general operation processor circuit to access the program data transferred into the programmable memory.

Claims 11-19 (Canceled).

20. (Previously Presented) A circuit for programming a monitor comprising:

a controller circuit configured to transfer program data from outside the monitor to a programmable memory in the monitor without using Random Access Memory (RAM) and Read Only Memory (ROM) devices that are separate from the controller circuit, the controller circuit being separate from a general operation processor circuit used to provide general operations of the monitor subsequent to transferring the program data into the programmable memory, the controller circuit being configured to transmit an indication to outside the electronic device that the transfer of program data to the programmable memory is complete;

a decoder circuit coupled to an interface via which the program data is transferred to the monitor, the decoder circuit configured to provide a first signal responsive to determining that data received via the interface includes an address within a programmable memory mapped address range and data to be programmed as specified in a head field and a command/address field data structure received by the decoder circuit without passing through the general operation processor circuit, the decoder circuit being further configured to assert a signal to the general operation processor circuit, responsive to decoding the programmable memory mapped address, to prevent the general operation processor circuit from accessing the programmable memory during transfer of program data into the programmable memory and configured to then de-assert the signal to the general operation processor circuit to allow the general operation processor circuit to access the programmable memory after the transfer of the program data to the programmable memory is complete; and

a buffer circuit coupled to the decoder circuit and the programmable memory and configured to store data provided to/from the programmable memory.

Claims 21-23 (Canceled).

24. (Previously Presented) The method according to Claim 1 wherein the step of transferring the program data further comprises transferring the program data via a Serial Interface to the electronic device.

25. (Previously Presented) The method according to Claim 1 further comprising:

cycling power provided to the controller circuit to reset the controller circuit to enable the general operation processor circuit to access the program data transferred into the programmable memory.

Claim 26 (Canceled).

27. (Previously Presented) The method according to Claim 1 wherein the buffer circuit comprises a programmable memory word or sector sized buffer circuit.

28. (Previously Presented) The circuit according to Claim 20 wherein the buffer circuit comprises a programmable memory word or sector sized buffer circuit configured to store word or sector amounts of data.